COUNTERS

Counter: It is a sequential circuit used for counting clock pulses. It calculates or note the no. of times an event has occurred. counter is the widely application of flip-flops. It is a group of flip-flops with a clock signal applied.

Types of counters:

Counters are basically of two types.

i) Asynchronous or ripple counter.

ii) Synchronous counters.

Asynchronous or Ripple counters- Asynchronous counters are those counter whose output is free from the clock signal. The required number of logic gate to design asynchronous counter is very less.

The another name of asynchrous counter is Ripple counters. The no. of flip-flop used in a ripple counter is depends upon the number of states of counter (ex: Mod 4, Mod 2 etc) The number of output states of counter is called Modulus or "MOD" of the counter. The maximum number of state that a counter can have is 2^n (where 'n' represents the number of flip-flop used in the counter.

eg: If we have 2 flip flops, the maximum number of outputs of counter is 4. So, it is called MOD-4 MOD-4 counter.

Types of counters

There are following types of Asynchronous counter available in digital electronics.

i) 2/4-bit synchronous up counter.

ii) 2/4-bit synchronous DOWN counter.

iii) 2/4-bit synchronous up/DOWN/ counter.

* For these counters, external clock signal is applied to one flip-flop and then output of preceding flip-flop is connected to the clock of next flip-flop.

① 2-BIT ASYNCHRONOUS COUNTER.

The below figure shows the logic diagram of a 2-bit ripple up counter. It consists of 2 flip-flops of T flip-flops

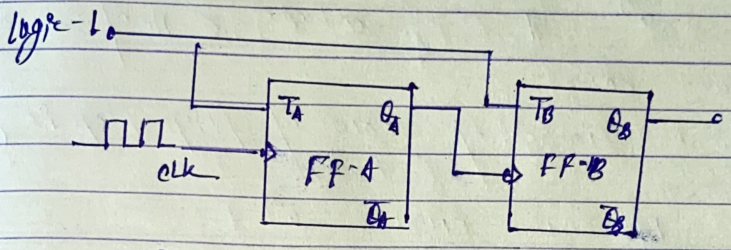

Fig: 2-bit asynchronous binary up counter.

working

Initially both the flip-flops are in reset condition. Therefore, $Q_B Q_A = 00$.

I) On the first negative falling edge, FF-A will toggle and $Q_A = 1$. Also, as Q_A is connected to the clock input of FF-B, since Q_A is $= 1$, there occurs is created a +ve clock pulse for FF-B and therefore, there is no change in Q_B. So, the state is

$$Q_B Q_A = 01$$

II) On the second negative falling edge of clock. FF-A toggle again and Q_A becomes 0, also Q_B toggles and Q_B becomes 1. i.e $Q_B = 1$. Therefore output is $Q_B Q_A = 10$.

III) On the third falling edge of clock, the o/p state is

~~$Q_B Q_A = 01$~~ $Q_B Q_A = 11$

IV) At the fourth Negative falling clock edge FF-A toggle and Q_A change from 1 to 0. This -ve change (Q_A) acts as clock pulse for FF-B it toggle to change Q_B from 1 to 0.

∴ $Q_B Q_A = 11$

Key points:

No. of states: Total no. of states of counter is 00, 01, 10, 11 is given by

$$2^n = 4$$ where n = No. of flip flops

II) Maximum count

Maximum number of count of flip-flop is given by

$$\text{Maximum count} = 2^n - 1$$

Truth Table:

clock	Outputs Q_B	Q_A	State Number
Initially	0	0	—
↓	0	1	1
↓	1	0	2
↓	1	1	3
↓	0	0	4

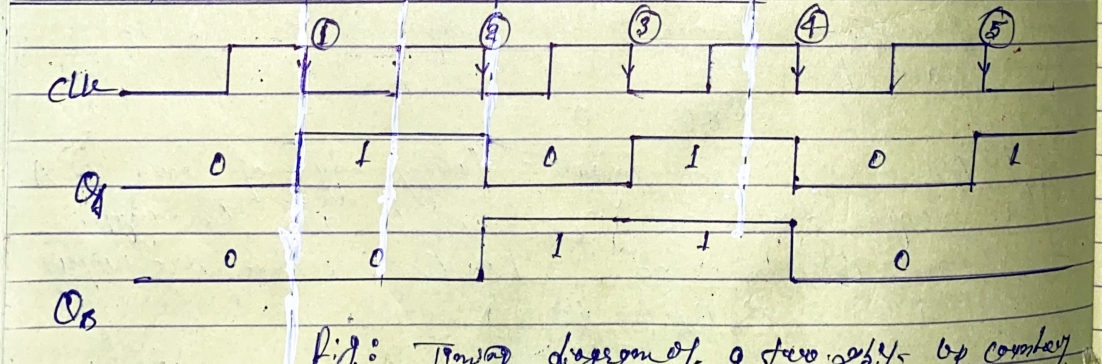

Fig: Timing diagram of a two bits by counter